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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	(check\$4 determin\$4 verif\$4) with floating with rotating adj registers	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:14
L2	4	(check\$4 determin\$4 verif\$4) same floating with rotating adj registers	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:14
L3	19	static adj register with rotating adj registers	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:14
L4	8	loop same (rotating adj register) same (spill\$4 fill\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:15
L5	12	pipe\$line with (rotating adj register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:16
L9	52	pipe\$line same floating same register same loop	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:16
L10	17	pipe\$line same (rotating adj register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:17
L11	65	loop same (rotating adj register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:18

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S1	2	"6651247".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/23 14:22
S2	14	(spill\$4 with fill\$4) with register with address	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/23 14:27
S4	27	(check\$4 determin\$4 verif\$4) with rotating adj registers	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 11:13


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Background engine performs **fill** and **spill** operations on. **register** stack ... **Register Stack**.

x86 Floating-point registers are organized as a **rotating** stack ...

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Optimal **spill** placement is less important. 16. **Register Spill** Problems. • no compiler cooperation. – **Rotating register** files. – ALAT for data speculation ...
 rogue.colorado.edu/EPIC4/presentations/2_robert_6pclr.pdf - [Similar pages](#)

Citations: Register allocation for software pipelined loops - Rau ...

Once the **register** allocation and **spill** is completed for R1, the algorithm ... Because this specific case of **rotating register** file allocation and ordinary ...

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Citations: Overlapped Loop Support in the Cydra - Dehnert, Hsu ...

Improved **Spill** Code Generation for Software Pipelined. ... A **rotating register** file can be used to solve this problem without replicating code by renaming ...

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Method, apparatus, and product for optimizing compiler with ...

(i) when the second **rotating register** is not available, inserting one or more **spill** code instructions in the first IR for the second live range, and ...

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Register Constrained Modulo Scheduling

A **rotating register** file can be used to solve this problem without replicating ... This is accomplished by scheduling the **spill** operation and its associated ...

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stack frame and **rotating register** base for GRs. The CFM holds the ... perform **register spill** and reload operations in the background when neces- ...

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Exposes **register** renaming to SW; Avoids **register spill** when few needed ... Separate **Rotating Register** Base for each: GRs, FRs, PRs; Loop branches decrement ...

www.es.ele.tue.nl/~heco/courses/aca/IA64/dale.ppt - [Similar pages](#)

HP OpenVMS systems documentation

The **rotating register** region always starts with R32, and may be any multiple ... This allows a procedure to **spill** its **register** parameters easily to memory ...

h71000.www7.hp.com/DOC/82FINAL/5841/5841pro_053.html - 45k -

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An Overview of the Intel IA-64 Compile

In IA-64, **rotating** predicates [5, 6, 7] are used to control the execution ... a basic block and is run after **register** allocation to schedule the **spill** code. ...

developer.intel.com/technology/itj/q41999/articles/art_1k.htm - 16k - [Cached](#) - [Similar pages](#)

CCCP: Trimaran Compiler Framework

... hardware support like predicates and **rotating register** files. ... coloring based **register** allocation algorithm. **Spill** code is introduced if necessary. ...

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Hardware conforming to IEEE Standard 754 for Binary **Floating-Point** does ... Sometimes compilers "**spill**" the contents of a wide **register** temporarily to a ...

www.cs.berkeley.edu/~wkahan/Mind1ess.pdf - [Similar pages](#)

[ia64 floating point - GCC Wiki](#)

The ia64 architecture's **floating point** has a number of exotic features: ... 'fill/**spill**' instructions that transfer the complete internal **register** content. ...

gcc.gnu.org/wiki/ia64%20floating%20point - 30k - [Cached](#) - [Similar pages](#)

Re: FLOATING-POINT CONSISTENCY, -FFLOAT-STORE, AND X86

Re: FLOATING-POINT CONSISTENCY, -FFLOAT-STORE, AND X86 ... but there was no efficient way to **spill** the full **register** width, nor would there have been much ...

gcc.gnu.org/ml/gcc/1998-12/msg00097.html - 13k - [Cached](#) - [Similar pages](#)

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Register Allocation

The integer and **floating point register** allocators are functors that only take client ...

spill/reload: are functions that describe how to **spill** and reload ...

cs.nyu.edu/leunga/www/MLRISC/Doc/html/mlrisc-ra.html - 12k - [Cached](#) - [Similar pages](#)

[LLVMbugs] [Bug 467] NEW: [X86] **Spill floating point stack values** ...

GCC takes the position that X86 **floating point** is already hopeless: many optimizations (eg **register** promotions, store-load forwarding, etc) hopelessly ...

lists.cs.uiuc.edu/pipermail/llvmbugs/2004-December/000972.html - 5k -

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Register Allocation

The results show that the **spill** heuristics and scratch **register** ... Mtrt degrades as we add more optimizations; however, the **floating-point** results here ...

www.usenix.org/event/jvm02/full_papers/alpern/alpern_html/node15.html - 11k -

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Lecture 4- CSC/MA 783 --Gary Howell Optimizing In-Cache Floating ...

This appears to be because we had **register spill** so that only about half of the instructions were **floating point** adds and multiplies (the rest being loads back ...

www.ncsu.edu/itd/hpc/Courses/4incache.html - 15k - [Cached](#) - [Similar pages](#)

Andrew Cagney - Re: MIPS o32 ABI spec, \$fp1 valid?

Does the o32 ABI specify how to **spill** a **floating point register** (a **spill** is ... Each even/odd pair of the 32 **floating-point** general registers can be used as ...

www.sourceware.org/ml/gdb/2003-06/msg00334.html - 7k - [Cached](#) - [Similar pages](#)

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Register set depends on the data-type. - **floating-point** values in **floating point** registers ... **Spill** the value to memory and load it back at the ...

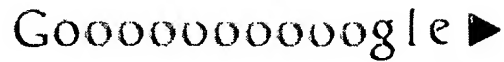
web.mit.edu/6.035/www/slides-2005/RegisterAllocation.pdf - [Similar pages](#)

HP OpenVMS systems documentation

The argument item sequence can have a mix of integer and **floating-point** items ... This allows a procedure to **spill** its **register** parameters easily to memory ...

<http://www.google.com/search?hl=en&lr=&q=floating+point+register+spill>

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